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# Mitigating the dead-time effects on harmonics spectrum of inverter waveform by the confined band VSFPWM technique

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**ABSTRACT**

The dead-time is necessary to be inserted between the gates drive pulses of the two power electronic switches in a one leg of any inverter to avoid a short circuit in the leg and the DC supply as well. However, adding the dead-time increases the low order harmonics of the output voltage/current waveform of the inverter. This paper investigates the positive effects of decreasing the pulse width modulation (PWM) drive pulses number per fundamental period on the current low order harmonics. In addition, this paper evaluates the impact of the confined band variable switching frequency pulse width modulation (CB-VSFPWM) technique on inverter performance in terms of dead-time mitigating, and consequenctely lowering the low order harmonics. CB-VSFPWM technique reduces the total harmonic distortion (THD) levels in the inverter output current as well. Theoretical analysis of the CB-VSFPWM effectiveness in reducing the negative effect of the dead-time has explained in this study and confirmed by the MATLAB/Simulink simulation results.



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## NOMENCLATURE

**Symbols**

| | |
|---|---|
| $f_C$ | Constant Switching Frequency, Carrier Frequency |
| $f_{VSF}$ | Variable Switching Frequency |
| $f_{CBVSF}$ | Confined Band Variable Switching Frequency |
| $B$ | Constant Parameter |
| $V_{DC}$ | DC link voltage |
| $f_{max}$ | Maximum frequency of variable switching frequency band |
| $f_{min}$ | Minimum frequency of variable switching frequency band |
| $T_d$ | dead time |
| $T_s$ | Switching period |
| $\omega$ | Reference frequency in rad/s |
| $V_{ref}$ | Fundamental reference voltage |
| $\Delta V$ | Average voltage deviation over a cycle (square wave) |

**Abbreviations**

| | |
|---|---|
| PWM | Pulse Width Modulation |
| VSFPWM | Variable Switching Frequency Pulse Width Modulation |
| CB-VSF | Confined Band Variable Switching Frequency |
| PWM | Pulse Width Modulation |
| THD | Total Harmonic Distortion |
| CSFPWM | Constant Switching Frequency Pulse Width Modulation |
| DC | Direct Current |
| VSI | Voltage Source Inverter |
| PWM | Pulse Width Modulation |

$\Delta V_1$ Amplitude of fundamental component of square wave ($\Delta V$)
$N_{PWM}$ Number of pulses per cycle
$T$ Time per cycle

## 1. INTRODUCTION

The two power switches in each column of a power electronic conversion system represent the core of the whole system. These switches are complementary connected and due to the difference between the rise time and the storage time, as well as the difference between the turn on time and turn off time, dead-time is necessary to be inserted to avoid the short circuit of the two transistors. To guantee enough ded-time duration, it needs to make sure the fully off state of a one transistor before turning on the second one of the same column [1]. However, inserting the dead-time negatively affects the low order harmonics levels and increases the distortion of the inverter output current waveform [2]-[10].

Many studies have been presented in analysing the effects of dead-time on the output voltage waveform and how compensate the dead-time. In the literature, there are two directions for the dead-time compensating; first one is by the voltage compensating through replacing the error voltage by an equally opposite voltage. The second direction of dead-time compensating is by calculating the error in the width of the generated pulse width modulation (PWM) pulses then replace this time error in the new width of the pulses [11]-[14].

The study of [11] have explained the dead-time effects on a three-phase voltage source inverter VSI voltage, and how to compensate the dead-time through the field oriented control (FOC) for a brushless motor [11].

The dead-time has different effect level depending on the generating scheme of PWM pulses [15]-[21]. In [15], the effect on the output reference frequency waveform, and the dead-time compensation have theoretically studied and experimentally investigated for bus-clamping PWM based inverter.

In the study of [16], a mathematical formulation and the discussion in terms of the harmonics spectrum of the PWM inverter voltage have presented.

A simple theoretical approach has presented in [17] for analyzing the effect of dead-time inserting in a three-phase inverter. The researchers in the study have focused on evaluating the output current ripple, shwoing the dead-time impact in distorting the output voltage.

The effect of dead-time has mitigated in [18] using a repetitive controller in a grid-tied converter system, the study outcomes reflected the priority of the presented solution compared to the traditional solution in terms of compensating the the dead-time, and how distortion of the low-order harmonics is mitigated. Comparing to the resonant controller, the repetitive controller of [18] have mitigated the dead-time effect without problem in system stability.

A solution of a virtual inductor has proposed in [19] to reduce the negative effects of a dead-time, and due to the virtual fact, there were no additional cost and losses. The way of designing the virtual inductor, the system sensitivity, stability, steady state error has discussed in the study, and concluded that the proposed solution can be effectively suppressed the dead-time effect when the inductor value is selected within an acceptable range, otherwise, the total harmonic distortion THD will be high.

A phase shift PWM technique for a three-level flying capacitor inverter is proposed in [20] for dead-time compensation. The solution of [20] have offered a simple algorithm for inserting a desired dead-time at turning-on and turning-off the connected power electronic switches without any distortion in the output voltage.

A new software method has proposed in [21] to evaluate the voltage error due to the dead-time. The error has monitored to calculate the suitable duty factor for controling the PWM modulator. The effectiveness of the [21] method has evaluated through comparing the simulation results with previously proposed methods at the same inverter setting.

Considering the reviewed studies in dead-time compensation, this paper proposes a mitigation method for the dead-time effect through the confined band variable switching frequency pulse width modulation CB-VSFPWM technique. The paper analyzes the effects of dead-time on the output voltage waveform of a single phase full-bridge inverter, inverter voltage harmonics spectrum, and the related parameters of the dead-time effect mitigating. The remaining of the paper are as follows: Section 2 shows the dead-time effect on the harmonics spectrum of the inverter waveform. The role of the CB-VSFPWM in mitigating the negative effects of the dead-time is shown in Section 3. A comparative simulation results with analysis for the function of a single phase inverter based on the presented CB-VSFPWM with respect to a traditional constant switching frequency pulse width modulation are shown in Section 4. The summary of the concluded points is shown in Section 5.

## 2. DEAD-TIME EFFECT ON HARMONIC SPECTRUM

The dead-time effect on inverter output voltage is shown in Figure 1 below. The dead-time affects the square wave amplitude of a fundamental frequency, and this increases the low order harmonics. The square signal is represented by the wave $\Delta V$, the fundamental frequency components is represented by the signal $V_{ref}$. The inverter output voltage includes frequency components of the square wave signal. The harmonics spectrum and THD are affected by the level of the sqare wave, and this level is dependent on the duration of the inserted dead-time [22]. The frequency components magnitude of the square wave voltage can be determined from (1).

$$V_n = \frac{1}{n}\Delta V_1 \quad n = 3,5,7 \ldots \tag{1}$$

where $\Delta V_1$ is the fundamental component of the square wave which can be found from (2).

$$\Delta V_1 = \frac{4}{\pi}\Delta V = \frac{4}{\pi}\left(\frac{N_{PWM}T_D}{T}V_{DC}\right) \tag{2}$$

where $N_{PWM}$ is the number of pulses per reference or fundamental cycle, $T$ is the full cycle time, $T_d$ is the dead-time, and $V_{DC}$ is the dc-link voltage.

From the above, the resultant harmonic distortion due to the dead time is proportional to the number of PWM drive pulses per reference cycle period, and the level of DC link voltage. In other words, increasing the number of dead-times per reference cycle, due to increasing the switching frequency of Constant Switching Frequency PWM, increases the square wave level and consequently increases the low order harmonics and harmonic spectrum in general.

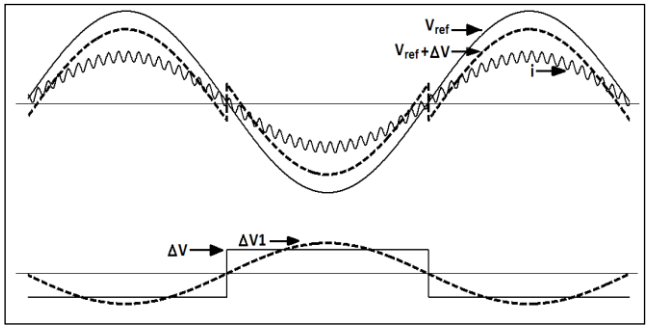



Figure 1. Dead-time effect of output voltage [22], [23]

## 3. CONFINED BAND VSFPWM FOR DEAD-TIME EFFECTS MITIGATION

Starting from tha fact of that the constant switching frequency PWM (CSFPWM) represents a common technique to generate the PWM drive pulses for different inverter types due to its simplicity. However, in the CSFPWM, to have low THD level, the switching frequency should be increased whereas inceasing the switching frequency increases the switching losses and reduces the system efficiency. At the same time, increasing the switching frequency increases the low order harmonics due to increasing the number of dead-times per reference cycle [24]-[26]. So, variable switching frequency PWM (VSFPWM) techniques have been proposed for flexible PWM pulses generation, and for improving THD level and switching losses as well [27]-[33].

Confined band VSFPWM (CB-VSFPWM) is currently proposed in [34], and [35] to simplify the design of the high order power filter, and to overcome the difficulties of the previous unconfined band VSFPWM techniques. These difficulties of the unconfined VSFPWM are represented by, firstly, the filter resonating possibility at low switching frequesies, and, secondly, the load current distorting possibility due to the pulse dropping if the varied switching frequency is exceeding the maximum limit of switching frequency.

The CB-VSFPWM technique in [34], and [35] have confined the switching frequency range within the desired band. The band can be limited between a minimum and a maximum switching frequency $f_{min}$ and $f_{max}$;

$$f_{max} = f_c \tag{3}$$
$$f_{min} = B \cdot f_c \; B \in [0,1] \tag{4}$$

where $f_c$ is the carrier frequency of CSFPWM , and $B$ is a constant parameter ($1 > B > 0$) which controls the width of the confined band. The CB-VSFPWM scheme becomes CSFPWM if $B$=1. In addition, the CB-VSFPWM offered the merits of enhancing the current harmonics spectrum, and total harmonic distortion THD, facilitating the filter design, and reducing the switching losses. Compared to the traditional CSFPWM technique, the CB-VSFPWM is mitigating the effects of dead-time by reducing the total number of PWM pulses per reference cycle period. Also CB-VSFPWM is selecting the location of the low frequency PWM pulses at the instants of high load current. The variation of the switching frequency through the CB-VSFPWM is illustrated in (5), and shown in Figure 2.

$$f_{CB-VSF} = fc \cdot \{1 - [(1 - B) \cdot abs(sin(\omega t))]\} \quad (5)$$

As shown in Figure 2, the switching frequency $f_{CB\text{-}VSF}$ is varying from the maximum frequency $f_{max}$ at the low voltage amplitude of the reference signal to the minimum frequency $f_{min}$ at the high voltage amplitude.

The switching frequency range can be limited in CB-VSFPWM within $B \bullet f_C < f_{CB\text{-}VSF} < f_C$, as shown in Figure 3 using the unipolar strategy of PWM pulses generation.

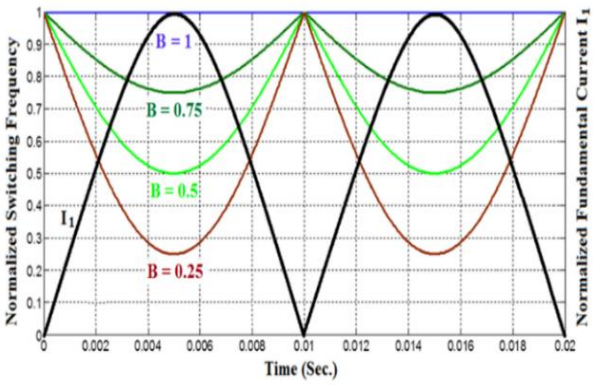



Figure 2. CB-VSFPWM technique for four values of B [34], [35]

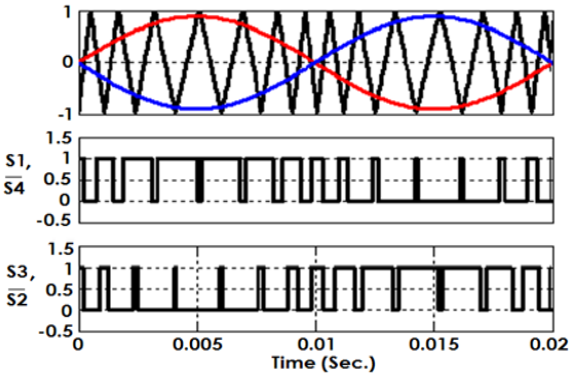



Figure 3. CB-VSFPWM with Unipolar strategy for a single phase inverter [34], [35]

From Figure 2, and Figure 3, the reduction of number of PWM pulses through the CB-VSFPWM is clearly noticeable compared to the CSFPWM. The pulses reduction definitely mitigates the dead-time effect, and consequentely, reduces the low order harmonic. At the same time, it reduces the switching losses by reducing the times of the turning on-off of the inverter switches.

## 4. ANALYSIS OF SIMULATION RESULTS

Single phase full bridge inverter is implemented via MATLAB/Simulink to evaluate the proposed CB-VSFPWM technique for dead-time effects mitigation. The proposed PWM technique is evaluated in terms of the harmonics spectrum and Total Harmonics Distortion THD on the inverter voltage waveform. Unipolar strategy is adopted in the presented comparative study. Firstly, the study shows the negative effects of dead-time increment on the inverter performance through a traditional constant switching frequency PWM (CSFPWM) at 20 kHz carrier frequency (the effective switching frequency is 40 kHz due to the unipolar strategy). Then, the inverter performance at the same parameter is evaluated via the confined band variable switching frequency PWM (CB-VSFPWM) using two switching frequency variation ranges, at $B$ = 0.25 or the carrier frequency variation is starting from 5 kHz to 20 kHz (the effective switching variation frequency is starting from 10 kHz to 40 kHz due to the unipolar strategy). The second variable switching frequency range at $B$ = 0.5 or the carrier frequency variation is starting from 10 kHz to 20 kHz (the effective switching variation frequency is starting from 20 kHz to 40 kHz due to the unipolar strategy). Table 1 shows the parameters setting of the implemented inverter for the two comparative PWM techniques (CSFPWM, and CB-VSFPWM).

Table 1. Inverter parameters

| Parameter | Value |
|---|---|
| Input dc link voltage, $V_{dc}$ | 400 V |
| Rated Power | 0.75 kW |
| PWM Strategy | Unipolar |
| Constant carrier frequency, $f_C$ | 20 kHz |
| CB-VSF carrier frequency range, $f_{CB\text{-}VSF}$ | 5 kHz to 20 kHz ($B$ = 0.25) |
| CB-VSF carrier frequency range, $f_{CB\text{-}VSF}$ | 10 kHz to 20 kHz ($B$ = 0.5) |
| DC-link capacitor | 2200 µF, 400 V |
| Resistive Load | 100 Ω |
| Modulation Index, m | 0.9 |

The simulation of the single phase full bridge inverter which is adopted in this study using the MATLAB/Simulink is shown in Figure 4. Due to the methodology of the selected unipolar strategy, the effective switching frequency is the double of the carrier frequency; Figure 5 shows the inverter performance based on the CSFPWM technique of carrier frequency 20 kHz and at two different dead-times 2.5 µsec and 5 µsec. The output voltage, the harmonics spectrum and THD level, all, are shown in Figure 5. From the zoom in of the low order harmonics, the low levels of the low order harmonis is demonstrated when inserting a low period of dead-time 2.5 µsec comparing to the a dead-time of 5 µsec. The negative effect of increasing the dead-time is noticeable if Figure 5 by Figure 5(a) with Figure 5(b) in terms of THD, low order harmonics spectrum and the levels of high order harmonics. Figure 6 shows the higher priority of the proposed CB-VSFPWM technique compared to the CSFPWM one in mitigating the negative effects of the dead-time on the inverter output voltage. Figure 6 shows the carrier frequency variation from 5 kHz to 20 kHz with respect to two dead-times, and indicates the effectiveness of the CB-VSFPWM in terms of this study obiectives. Figure 7 shows the inverter output voltage of another carrier frequency variation starting from 10 kHz to 20 kHz. Figure 7 again confirms the effectiveness of the CB-VSFPWM in terms of mitigation the dead-time effects, enhancing the harmonics spectrum and THD level as well.

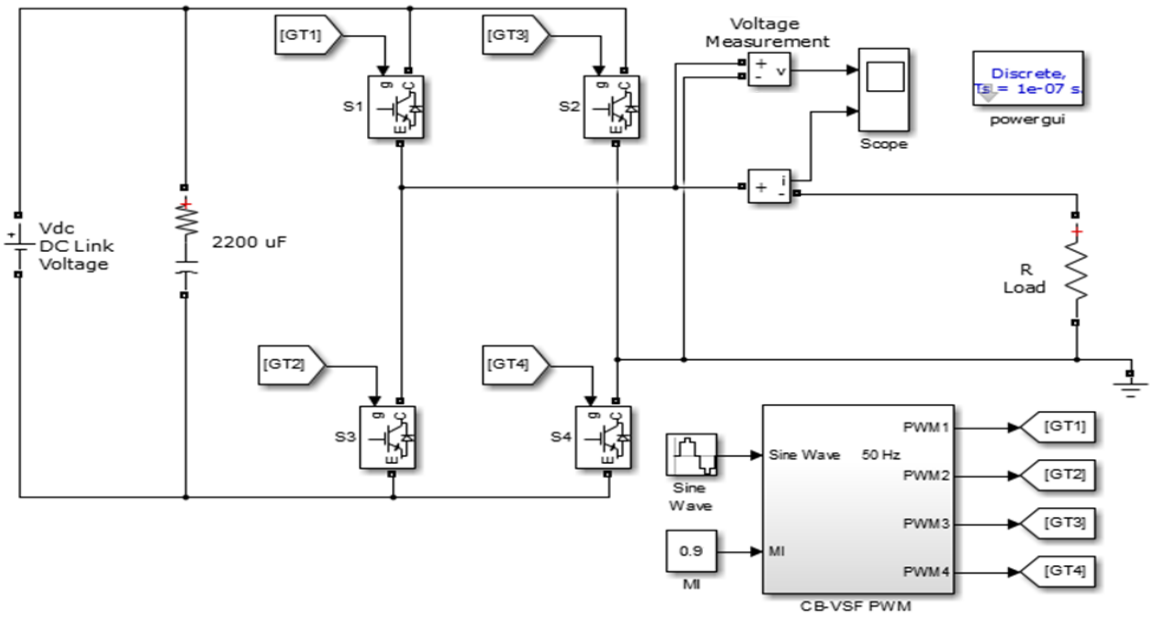



Figure 4. The single phase full bridge inverter based on PWM unipolar scheme for CSFPWM and CB-VSFPWM techniques.

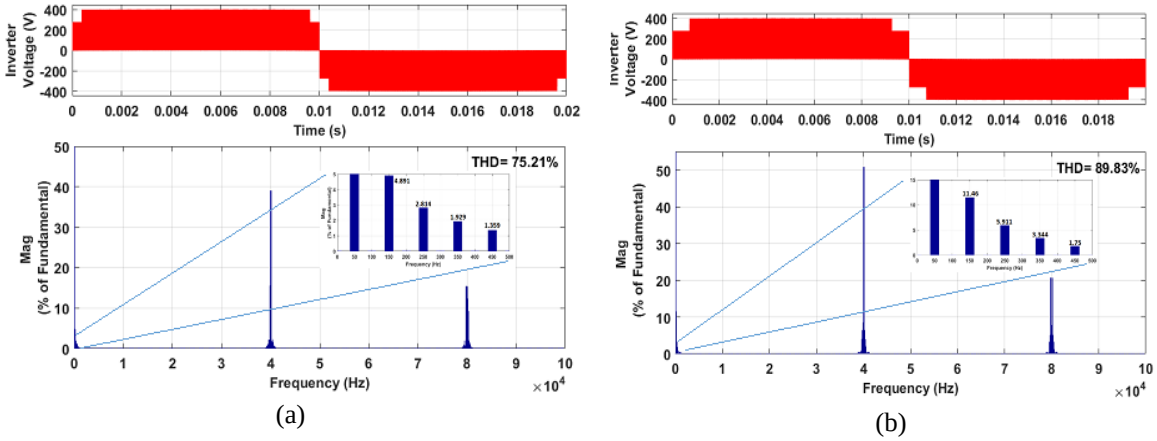



Figure 5. The inverter output voltage with the harmonics spectrum and THD level via unipolar CSFPWM technique (fc = 20 kHz); (a) Dead-time Td = 2.5 µsec, (b) Dead-time Td = 5 µsec

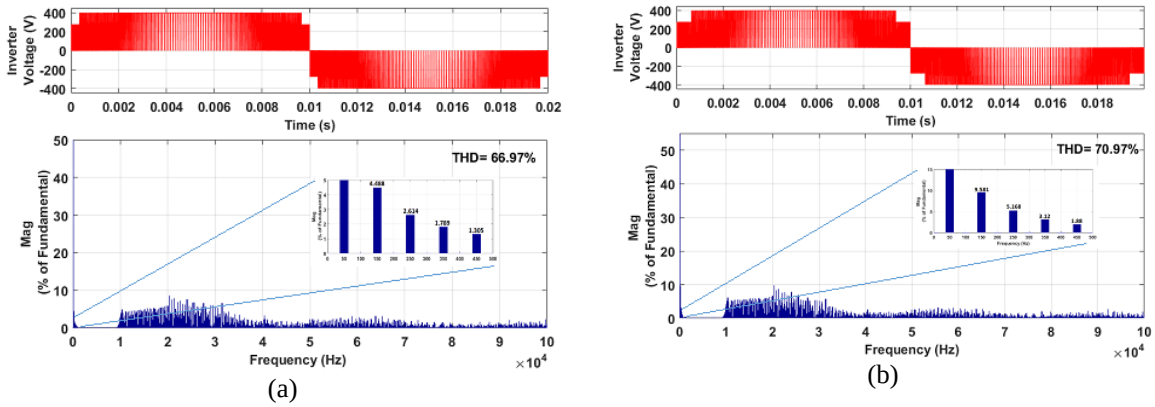



Figure 6. The inverter output voltage with the harmonics spectrum and THD level via unipolar CB-VSFPWM technique (fc = 5 kH to 20 kHz); (a) Dead-time Td = 2.5 µsec, (b) Dead-time Td = 5 µsec.

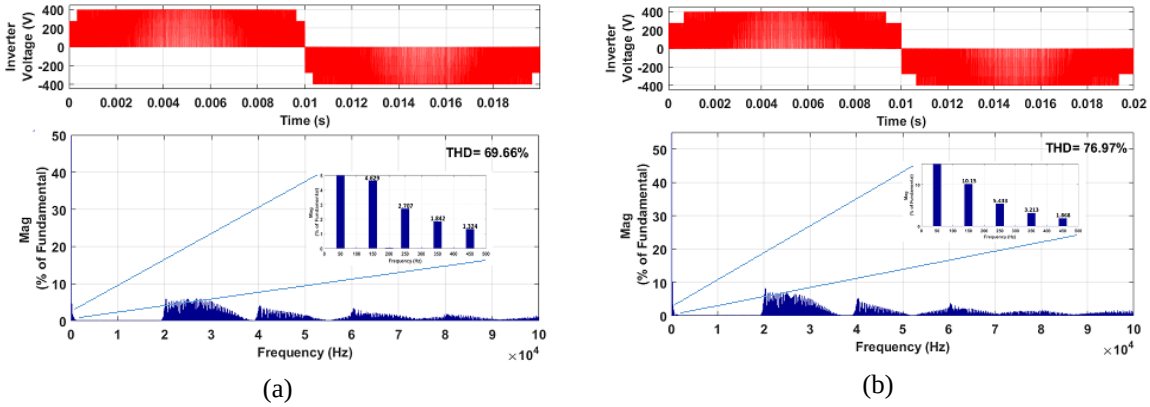


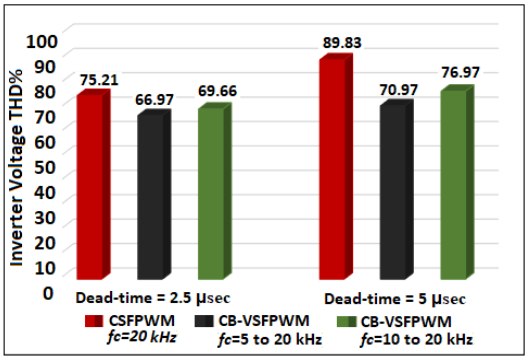

Figure 7. The inverter output voltage with the harmonics spectrum and THD level via unipolar CB-VSFPWM technique (fc = 10 kH to 20 kHz); (a) Dead-time Td = 2.5 µsec, (b) Dead-time Td = 5 µsec.

Table 2 summarizes the levels of the low order harmonics and THD for the two comparative PWM techniques; CSFPWM and CB-VSFPWM. Figure 8(a) shows the THD levels for the CSFPWM of 20 kHz, and the two confined bands of CB-VSFPWM, whereas Figure 8(b) shows the low order harmonics.

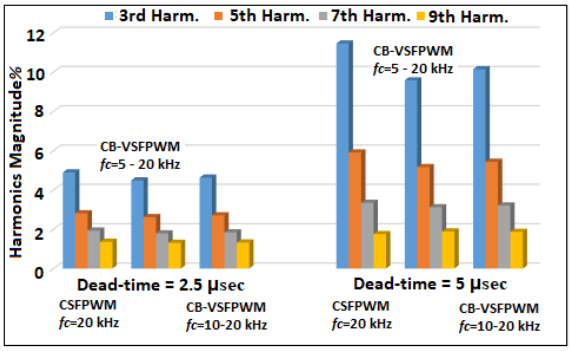
From the above theoretical analysis, and simulation results, the higher priority of the proposed CB-VSFPWM technique is clearly noticeable.

Table 2. Inverter performance: comparative results

| PWM Technique | THD % | 3rd order Harmonic | 5th order Harmonic | 7th order Harmonic | 9th order Harmonic |
|---|---|---|---|---|---|
| CSFPWM (20 kHz, Td = 2.5 µsec) | 75.21% | 4.891 | 2.814 | 1.929 | 1.359 |
| CSFPWM (20 kHz, Td = 5 µsec) | 89.83% | 11.46 | 5.911 | 3.344 | 1.75 |
| CB-VSFPWM (5 – 20 kHz, Td = 2.5 µsec) | 66.97% | 4.488 | 2.614 | 1.789 | 1.305 |
| CB-VSFPWM (5 – 20 kHz, Td = 5 µsec) | 70.97% | 9.581 | 5.168 | 3.12 | 1.888 |
| CB-VSFPWM (10 – 20 kHz, Td = 2.5 µsec) | 69.66% | 4.629 | 2.707 | 1.842 | 1.324 |
| CB-VSFPWM (10 – 20 kHz, Td = 5 µsec) | 76.97% | 10.15 | 5.433 | 3.213 | 1.868 |




(a)




(b)

Figure 8. Comparative analysis considering two dead-times via CSFPWM and CB-VSFPWM schemes (a) THD% of inverter output voltage, (b) Low order harmonics.

## 5. CONCLUSION

This paper investigated the impact of the confined band variable switching frequency pulse width modulation CB-VSFPWM in mitigating the dead-time effects on the low order harmonics and THD levels of the PWM inverter output waveform. The paper, firstly, presented the principle of the CB-VSFPWM technique, and demonstrated the theoretical analysis about the effectiveness of this technique in mitigating the effects of dead-time. The inverter performance is evaluated in compative way between the traditional CSFPWM technique and the CB-VSFPWM technique in terms of the low order harmonics levels, harmonics spectrum and THD percentages. The study adopted the MATLAB/Simulink to simulate a single phase full bridge inverter, and generated the required PWM drive pulses via unipolar strategy for the two PWM schemes. The study, through a comparative analysis, demonstrated the effectiveness of the confined band VSFPWM technique in mitigating the effects of dead-time.

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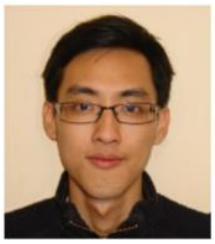

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